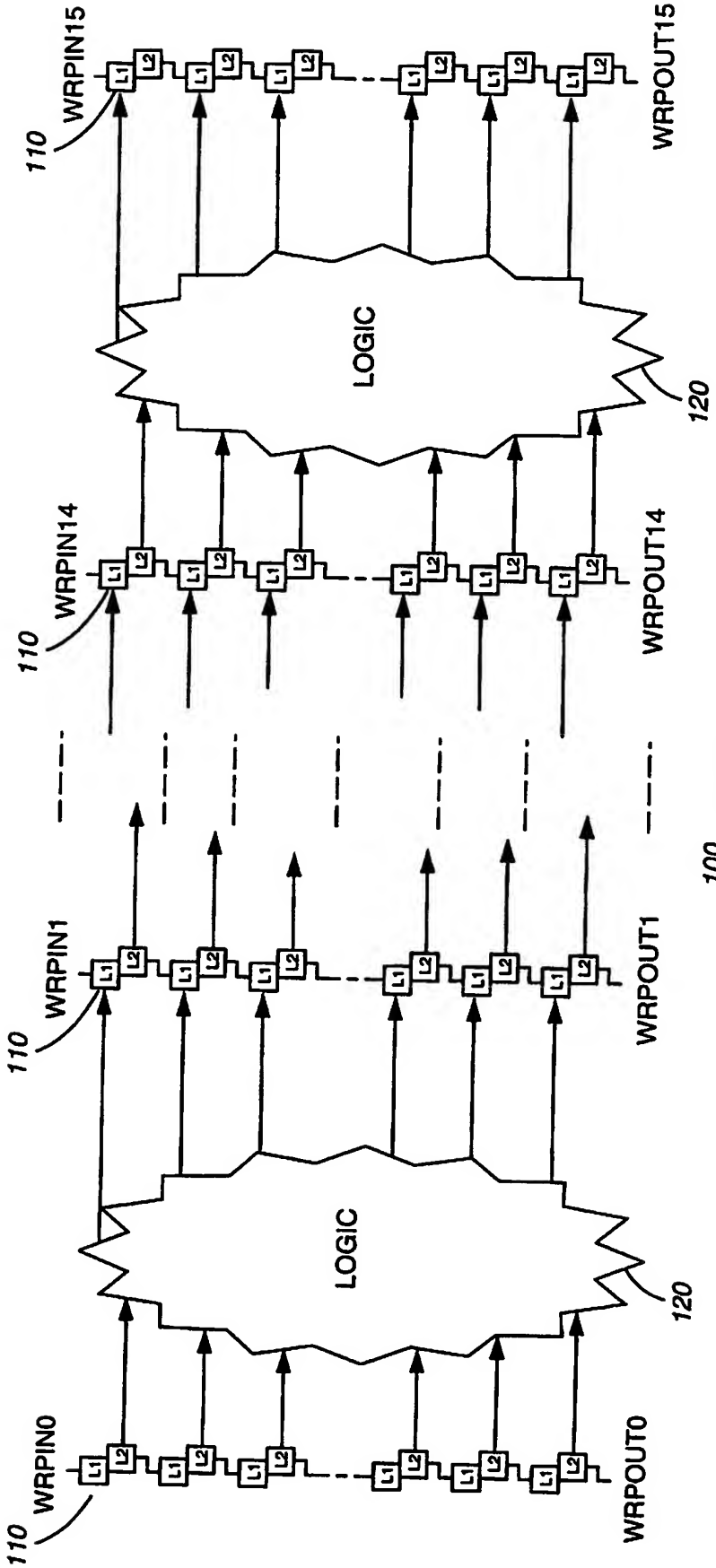


FIG. 1 PRIOR ART

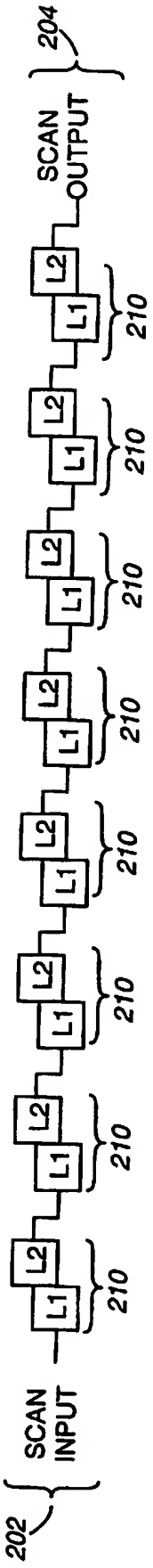
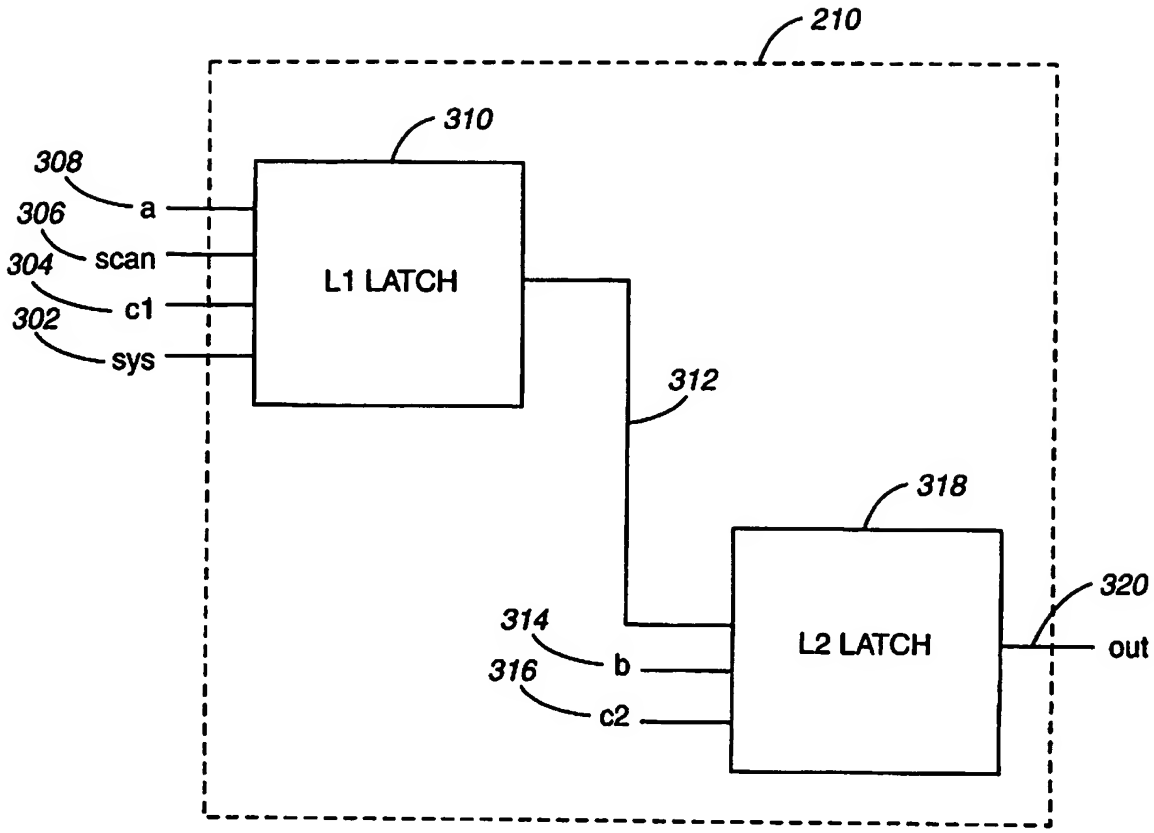
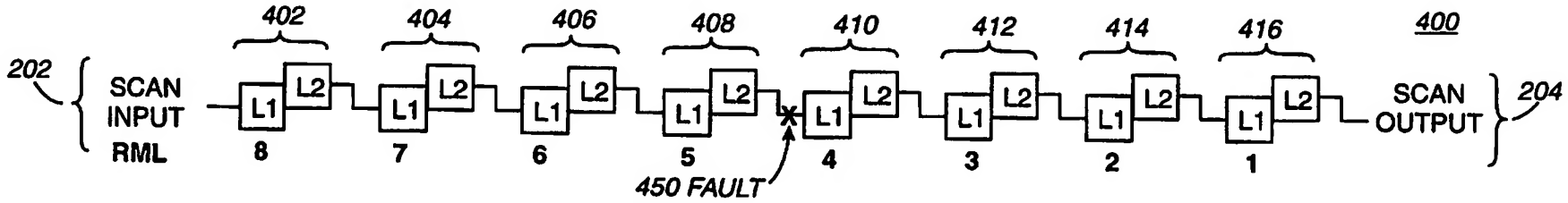


FIG. 2 PRIOR ART



PRIOR ART

FIG. 3



CYCLE

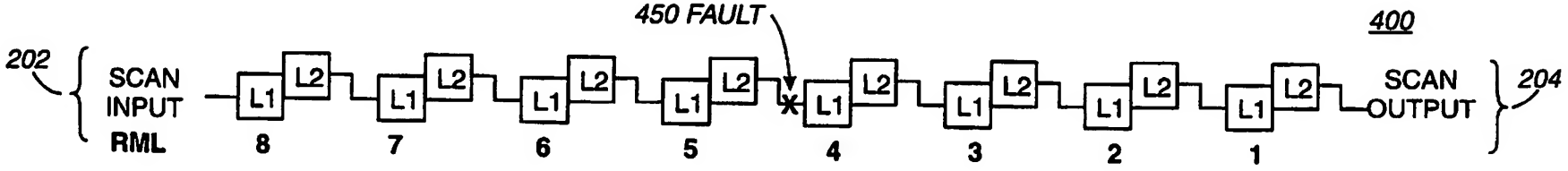
0	?	?	?	?	?	?	?	?	LOAD ALL ZERO'S IN OPERATING REGION
1	0	?	?	?	?	?	?	?	
2	0	0	?	?	?	?	?	?	
420 3	0	0	0	?	?	?	?	?	
4	0	0	0	0	?	?	?	?	
5	0	0	0	0	0	?	?	?	
6	0	0	0	0	0	0	?	?	
7	0	0	0	0	0	0	0	?	
8	0	0	0	0	0	0	0	0	

CYCLE

0	0	0	0	0	0	0	0	0	UNLOAD IN FAILING REGION
1	0	0	0	0	1	0	0	0	
2	0	0	0	0	1	1	0	0	
422 3	0	0	0	0	1	1	1	0	
4	0	0	0	0	1	1	1	1	
5	0	0	0	0	1	1	1	1	
6	0	0	0	0	1	1	1	1	PRIOR ART
7	0	0	0	0	1	1	1	1	

FIG. 4

Todd Michael Burdine et al.
ROC920030281US1



CYCLE									
	0	?	?	?	?	?	?	?	?
	1	0	?	?	?	?	?	?	?
	2	0	0	?	?	?	?	?	?
520	3	0	0	0	?	?	?	?	?
	4	0	0	0	0	?	?	?	?
	5	0	0	0	0	1	?	?	?
	6	0	0	0	0	1	1	?	?
	7	0	0	0	0	1	1	1	?
	8	0	0	0	0	1	1	1	1

LOAD ALL ZERO'S IN FAILING REGION

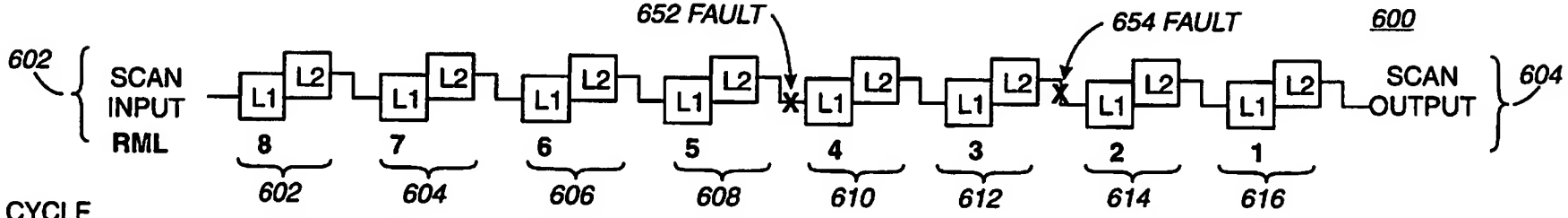
CYCLE									
	0	0	0	0	0	1	1	1	1
	1	0	0	0	0	0	1	1	1
	2	0	0	0	0	0	0	1	1
522	3	0	0	0	0	0	0	0	1
	4	0	0	0	0	0	0	0	0
	5	0	0	0	0	0	0	0	0
	6	0	0	0	0	0	0	0	0
	7	0	0	0	0	0	0	0	0

UNLOAD IN OPERATING REGION

PRIOR ART

FIG. 5

Todd Michael Burdine et al.
ROC920030281US1



CYCLE									
	0	?	?	?	?	?	?	?	?
	1	0	?	?	?	?	?	?	?
	2	0	0	?	?	?	?	?	?
620	3	0	0	0	?	?	?	?	?
	4	0	0	0	0	?	?	?	?
	5	0	0	0	0	0	?	?	?
	6	0	0	0	0	0	0	?	?
	7	0	0	0	0	0	0	0	?
	8	0	0	0	0	0	0	0	0

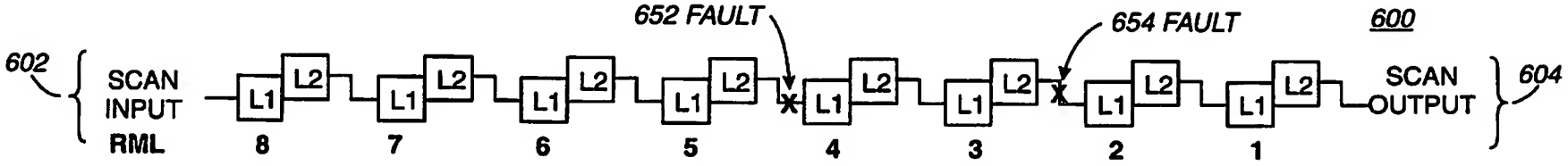
LOAD ALL ZERO'S IN FAILING REGION

CYCLE									
	0	0	0	0	0	0	0	0	0
	1	0	0	0	0	1	0	1	0
	2	0	0	0	0	1	1	1	1
622	3	0	0	0	0	1	1	1	1
	4	0	0	0	0	1	1	1	1
	5	0	0	0	0	1	1	1	1
	6	0	0	0	0	1	1	1	1
	7	0	0	0	0	1	1	1	1

UNLOAD IN OPERATING REGION

PRIOR ART

FIG. 6



720

CYCLE									
0	?	?	?	?	?	?	?	?	LOAD ALL ZERO'S IN FAILING REGION
1	0	?	?	?	?	?	?	?	
2	0	0	?	?	?	?	?	?	
3	0	0	0	?	?	?	?	?	
4	0	0	0	0	?	?	?	?	
5	0	0	0	0	1	?	?	?	
6	0	0	0	0	1	1	?	?	
7	0	0	0	0	1	1	0	?	
8	0	0	0	0	1	1	1	1	

722

CYCLE									
0	0	0	0	0	1	1	1	1	UNLOAD IN OPERATING REGION
1	0	0	0	0	0	1	1	1	
2	0	0	0	0	0	0	1	1	
3	0	0	0	0	0	0	0	1	
4	0	0	0	0	0	0	0	0	
5	0	0	0	0	0	0	0	0	
6	0	0	0	0	0	0	0	0	PRIOR ART
7	0	0	0	0	0	0	0	0	

FIG. 7

Todd Michael Burdine et al.
ROC920030281US1

10/767,046

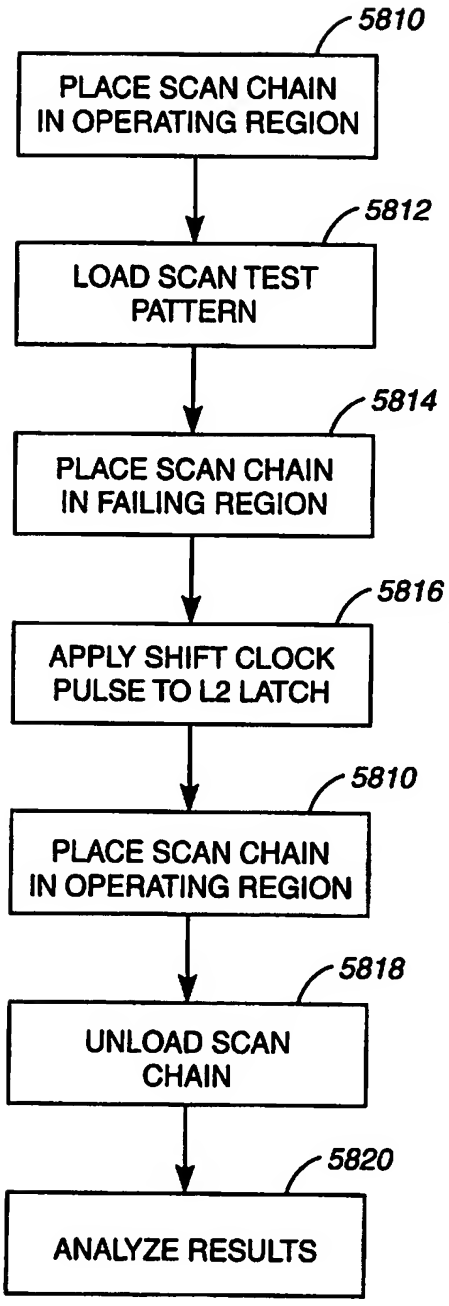

5810
PLACE SCAN CHAIN IN OPERATING REGION
5812
LOAD SCAN TEST PATTERN
5814
PLACE SCAN CHAIN IN FAILING REGION
5816
APPLY SHIFT CLOCK PULSE TO L2 LATCH
5810
PLACE SCAN CHAIN IN OPERATING REGION
5818
UNLOAD SCAN CHAIN
5820
ANALYZE RESULTS

FIG. 8

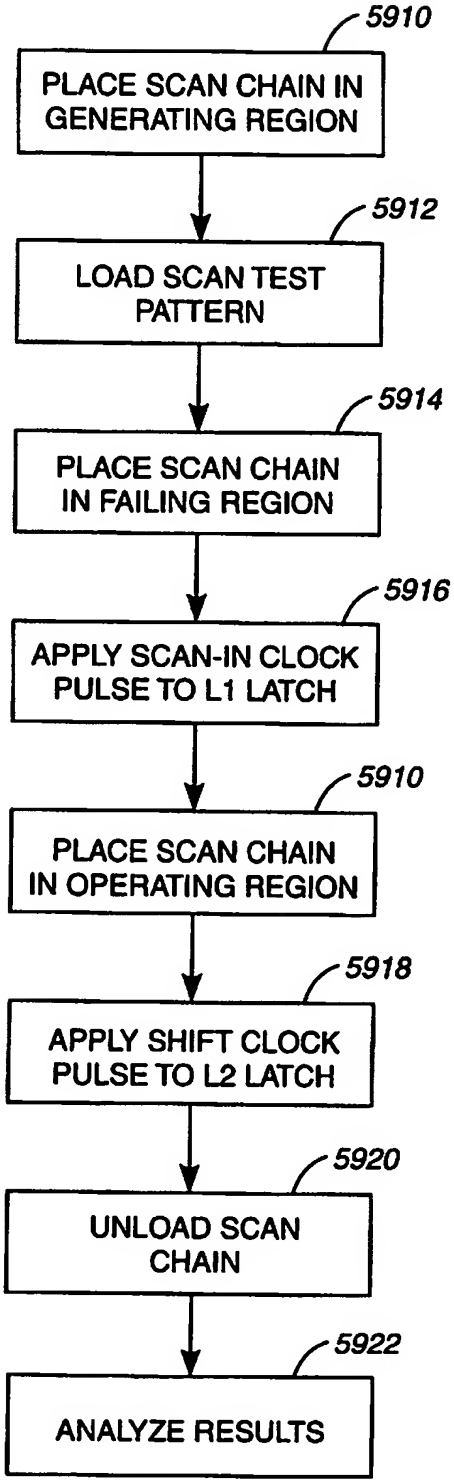
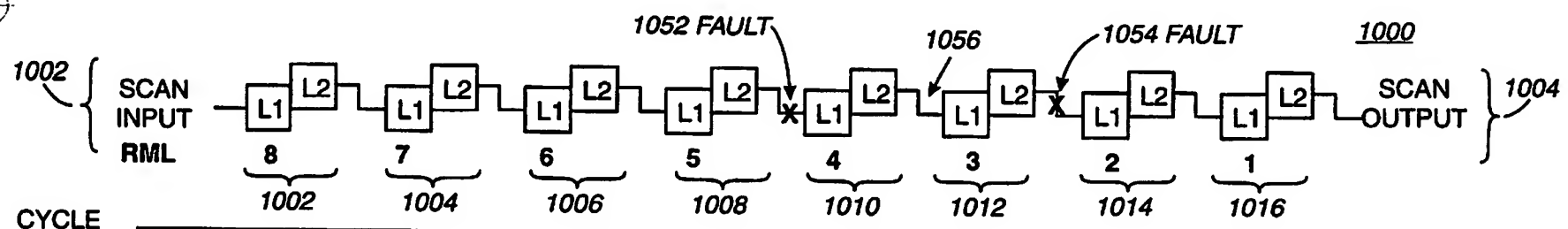

5910
PLACE SCAN CHAIN IN GENERATING REGION
5912
LOAD SCAN TEST PATTERN
5914
PLACE SCAN CHAIN IN FAILING REGION
5916
APPLY SCAN-IN CLOCK PULSE TO L1 LATCH
5910
PLACE SCAN CHAIN IN OPERATING REGION
5918
APPLY SHIFT CLOCK PULSE TO L2 LATCH
5920
UNLOAD SCAN CHAIN
5922
ANALYZE RESULTS

FIG. 9



CYCLE								
0	?	?	?	?	?	?	?	?
1	0	?	?	?	?	?	?	?
2	0	0	?	?	?	?	?	?
1020 3	0	0	0	?	?	?	?	?
4	0	0	0	0	?	?	?	?
5	0	0	0	0	0	?	?	?
6	0	0	0	0	0	0	?	?
7	0	0	0	0	0	0	0	?
8	0	0	0	0	0	0	0	0

LOAD ALL ZERO'S IN FAILING REGION

CYCLE								
1024 1	0	0	0	0	1	1	1	0

APPLY SCAN CLOCK A (SCANNING CLOCK) IN FAILING REGION

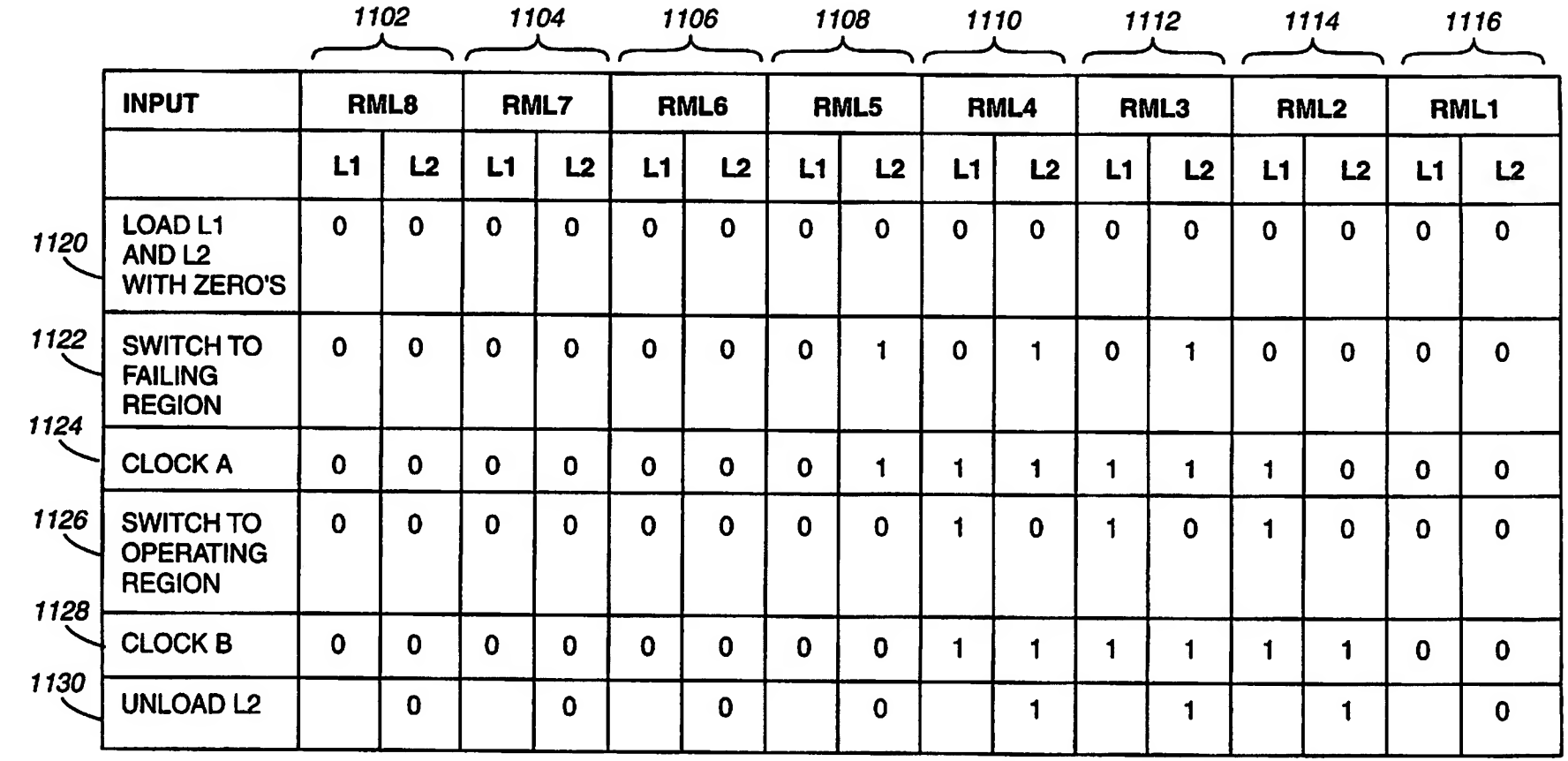
CYCLE								
0	0	0	0	0	1	1	1	0
1	0	0	0	0	0	1	1	0
2	0	0	0	0	0	0	1	1
1022 3	0	0	0	0	0	0	0	1
4	0	0	0	0	0	0	0	1
5	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0

UNLOAD IN OPERATING REGION

FIG. 10

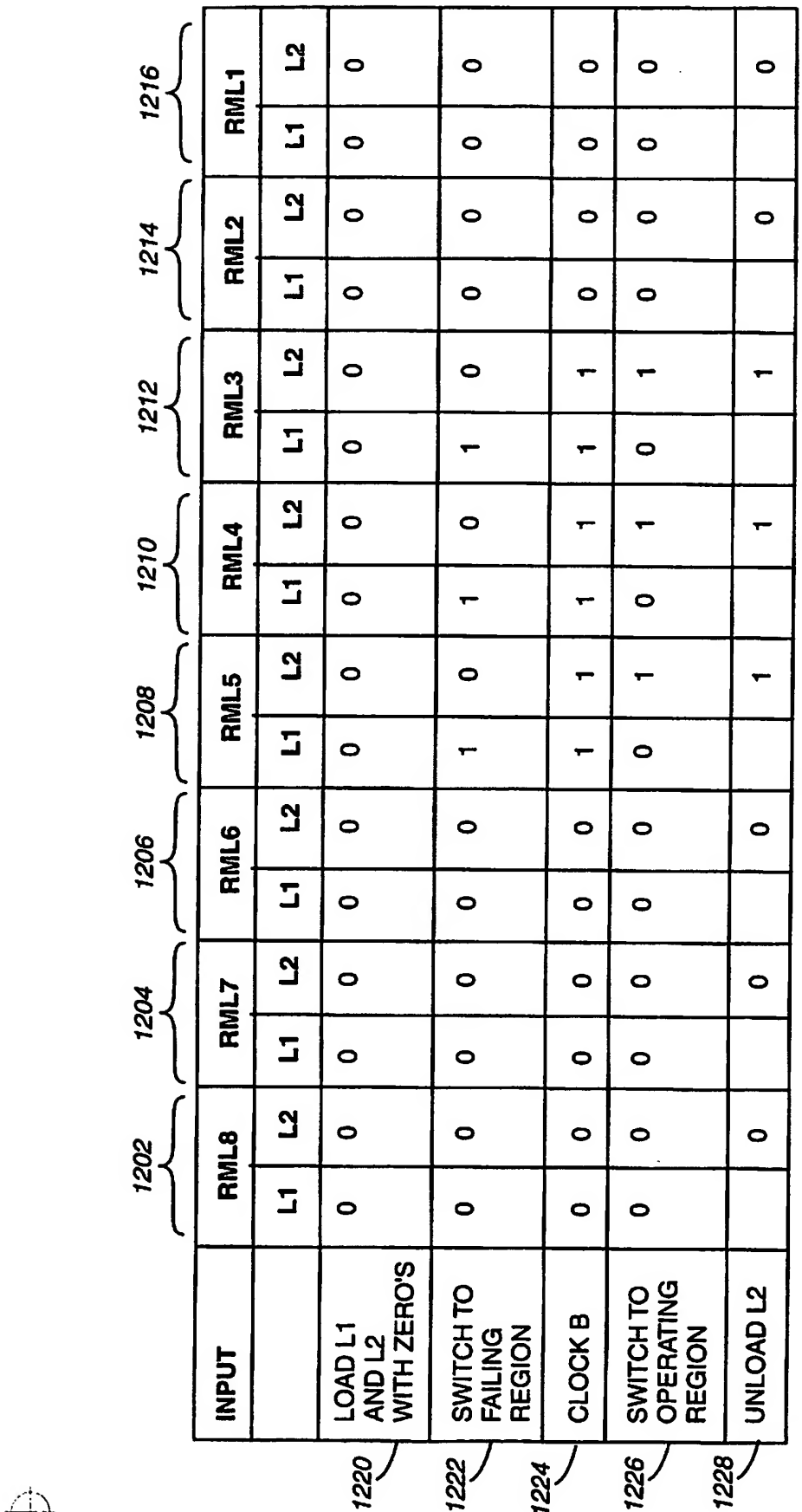
Todd Michael Burdine et al.
ROC920030281US1

REPLACEMENT SHEET
10/767,046



	INPUT	RML8		RML7		RML6		RML5		RML4		RML3		RML2		RML1	
		L1	L2	L1	L2	L1	L2	L1	L2	L1	L2	L1	L2	L1	L2	L1	L2
1120	LOAD L1 AND L2 WITH ZERO'S	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1122	SWITCH TO FAILING REGION	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0
1124	CLOCK A	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0
1126	SWITCH TO OPERATING REGION	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
1128	CLOCK B	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1130	UNLOAD L2		0		0		0		0		1		1		1		0

FIG. 11 1100



	INPUT	RML8		RML7		RML6		RML5		RML4		RML3		RML2		RML1	
		L1	L2	L1	L2	L1	L2	L1	L2	L1	L2	L1	L2	L1	L2	L1	L2
1220	LOAD L1 AND L2 WITH ZERO'S	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1222	SWITCH TO FAILING REGION	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0
1224	CLOCK B	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
1226	SWITCH TO OPERATING REGION	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0
1228	UNLOAD L2		0		0		0		1		1		1		0		0

1202 1204 1206 1208 1210 1212 1214 1216

FIG. 12 1200